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3D Tri-Gate Transistor Technology and Next Generation FPGAs

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Abstract

The 3D tri-gate transistors are a remarkable breakthrough in the realm of CMOS technology. These transistors can be considered as a reinvention of the transistor, in a way that they have supplanted the conventional "flat" 2D planar gate with an incredibly thin 3D silicon fin that rises up vertically from the silicon substrate. Such tri-gate transistors have shown significantly improved electrostatics in terms of sub-threshold slope and drain induced barrier lowering and hence better more scalability than planar transistors. This next-generation technology, which targets ultra high-performance systems for military, wire line communications, cloud networking, and compute and storage applications, will enable breakthrough levels of performance and power efficiencies not otherwise possible. These tri-gate transistors in concert with other key semiconductor technologies will enable a new era of energy-efficient performance. This Paper discusses the 3-D Tri-Gate transistor technology, its developments and integration with other silicon processing technologies, and its impact on the next generation FPGAs based on it.

Keywords: MOSFET, CMOS, FPGA, 3D tri-gate transistors, FinFET, DELTA.

Introduction

Tri-gate transistor is a MOSFET (metal-oxide-semiconductor field effect transistor) which incorporates three gates into a single device. It is a type of multiple gate field effect transistors (MuGFET). The three gates may be controlled by a single gate electrode, wherein the three gate surfaces act electrically as a single gate, or they can be operated independently.

For over 50 years, integrated circuits were using planar transistors as its core, during this period the size of the individual transistors has steadily decreased. Today, the transistor gate length in production is approximately 28 nanometres. But there are several limitations or drawbacks of these miniaturisations, most significant are: excessive gate leakage current, exponentially increasing source to drain sub-threshold leakage current, gate stack reliability and channel mobility degradation from increasing electric field, rising dynamic power dissipation ($CV2f$) from non-scaled supply voltages, band to band tunnelling leakage at high body doping levels, device to device variation from random dopant fluctuation effects.

Compared to today's 65nm transistors, integrated tri-gate transistors can offer a 45 percent increase in drive current (switching speed) or 50 times reduction in off-current, and 35 percent reduction in transistor switching power.

At present, Intel Corporation is the only company to have made this design and manufacturing transition in 22 nm technology, and can provide data on

the overall maturity and manufacturability of Tri-Gate transistors on a mass production scale. In February 2013, ALTERA and Intel Corporation jointly announced that the next generation of ALTERA's highest performance FPGA products would be manufactured using Intel's 14 nm 3-D Tri-Gate transistor technology exclusively. Next generation FPGAs based on 14 nm Tri-Gate design will enjoy benefits from both, the transistor geometry shrink to 14 nm and from further density improvements allowed by 3-D Tri-Gate transistor design.

History and Development of 3D TRI-Gate Technology

For over 50 years, MOSFET possessed the 2D planar structure in which the current was flowing along the surface of the silicon under the gate. In the last decade, advancements in strained silicon and High-K metal gate technologies have paved out continuous improvements in MOSFET performance and power.

The 3D tri-gate technology (also known as 'wraparound' gate transistor technology) was conceived in the year 1991. It was in this year when its potential and capabilities were acknowledged by scientists. This proposed 3-D structure was called 'depleted lean-channel transistor', or DELTA.

In 1997, the Defence Advanced Research Projects Agency (DARPA) awarded a contract to a research group at the University of California, Berkeley,

to develop a deep sub-micron transistor based on the DELTA concept.

In 1999, the 3D transistor was called 'FinFET' for the fin-like structure at the centre of the transistor geometry.

In 2002, to address the transistor off-state leakage issue, Intel developed the world's first CMOS tri-gate transistor, which employed a novel three-dimensional gate design that improves the drive current while reducing the leakage current when the transistor is in the off state. Intel has further improved the performance and energy efficiency of the transistor by integrating the tri-gate design with other silicon process technology and material innovations, including strained silicon, high-k gate dielectrics, metal gate electrodes, and epitaxially raised source/drain.

On 4th May 2011, Intel Corporation proclaimed their Tri-Gate transistor design that had been selected for the design and manufacture of their 22 nm semiconductor products.

It represented a solid acknowledgment of the feasibility and cost-effectiveness of the Tri-Gate transistor structure in semiconductor production.

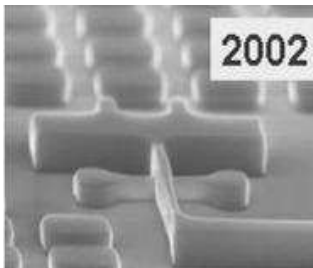


Fig.1 Single-fin Transistor

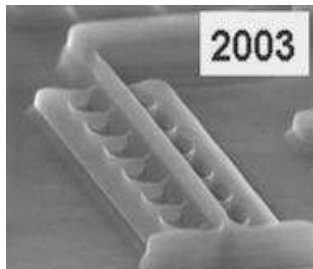


Fig2 Multi-fin Transistor

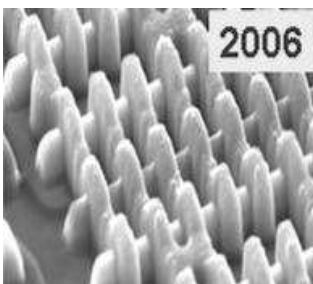


Fig3 Tri-gate SRAM cells

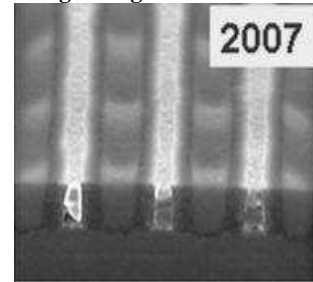


Fig 4 Tri-gate RMG process flow

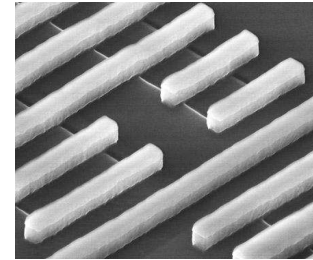


Fig.5 32 nm Planar Transistors

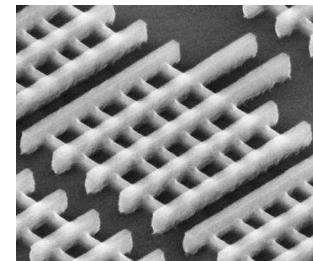


Fig.6 22 nm Tri-Gate Transistors

2011

Basic Structure of TRI-Gate Transistors

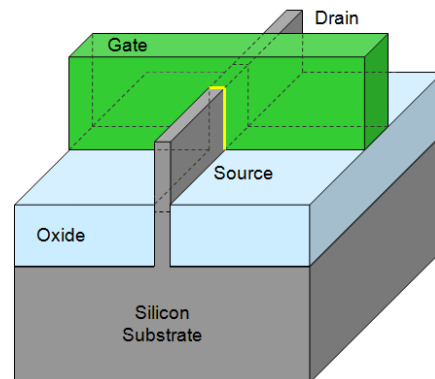


Fig.7 Structure of 3D Tri-Gate

The structure of 3D Tri-gate transistor represents a fundamental departure from the 2D planar transistor structure as shown in Fig.7. Tri-gate transistors form conducting channels on three sides of a vertical fin structure, thus they are fully depleted so that the entire available silicon underneath the gate electrode is

depleted of carriers before the threshold condition is reached.

Since fins are made vertical in nature, high packing density can be achieved, by packing transistors closer together. Further, to get even more performance and energy-efficiency gains, designers also have the ability to continue growing the height of the fins.

Tri gate transistor can be fabricated either on the SOI substrate or standard bulk-silicon substrate. It has one gate electrode on the top and other two gate electrodes on the sides of the silicon body. This additional gate control enables as much transistor current flowing as possible when the transistor is in the 'on' state (for performance), and as close to zero as possible when it is in the 'off' state (to minimize power), and enables the transistor to switch very quickly between the two states (again, for performance).

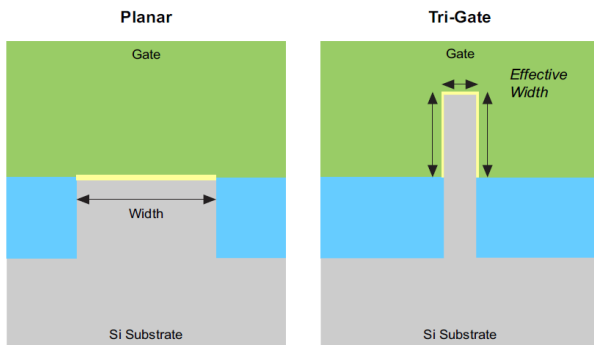


Fig.8 Planar Structure

Fig.9 Tri-gate Structure

The key performance advantage of Tri-Gate transistor geometries over traditional planar geometries can be found in the effective width of the conducting channel.

Figure 8 shows a cross-sectional representation of a traditional transistor. Its gate is built in a single plane (thus the name “planar”). The effective width of the channel is shown in yellow. Fig.9 shows a 3D tri-gate transistor, demonstrating how a greater channel width is achieved from the 3-D structure without increasing the overall footprint of the transistor, which results in higher performance without increased die area.

Without any impact on the layout area, designers have a choice of extending the width in third dimension in tri gate transistor structure; as a result the effective channel width can be significantly enhanced relative to a planar transistor.

Effective channel length and the effective fin width of the device are used as the key knob for controlling the short channel effects in 3D transistors. Device designers design electro-statically well controlled 3D transistors by keeping the effective channel length to

fin width ratio greater than 0.5. This also allows them to reduce the channel doping which, in turn, reduces the impurity scattering the channel, enhances volume inversion effect and results in higher performance, particularly at lower bias region.

Besides these advantages, there are several known issues and characteristics of the 3-D gate structure, which include the modelling of new parasitic capacitance values not modelled in traditional planar designs, layout dependent effects, and the use of double-patterning techniques using current lithographic equipment to form closely spaced fins.

Integration of TRI-Gate design with Other Technologies

For improving the efficiency, the tri-gate design is enhanced by using both high-k gate insulators with metal gates to improve both on and off currents, and adding strained silicon for enhanced mobility (speed), further improving device performance.

Non-planar transistor integrated with other silicon process technologies can provide 30 percent higher NMOS drive current and 60 percent higher PMOS drive current than the optimized, state-of-the-art 65nm-node planar transistors at the same off-state leakage.

Strain Modulation

Strain Modulation is a silicon process technology used in planar CMOS for improving their performance. Now, Intel is combining the benefits of non-planar fully depleted tri-gate architecture with strain engineering. Modulation of strain in transistor channel enhances electron mobility and hole mobility and thereby conductivity through the channel.

One key consideration in using strain engineering in CMOS technologies is that PMOS and NMOS respond differently to different types of strain. Specifically, PMOS performance is best served by applying compressive strain to the channel, whereas NMOS receives benefit from tensile strain.

High-k/metal gate Technology

The term high-k dielectric refers to a material with a high dielectric constant as compared to silicon dioxide. The tri-gate CMOS transistors use a high-k material to replace the transistor's traditional silicon dioxide dielectric, and also replace the conventional poly-silicon gate electrode with metal gate electrodes with work function close to the mid gap. Replacing the silicon dioxide gate dielectric with a high- κ material allows increased gate capacitance without the associated leakage effects.

The metal gate technology eliminates poly-silicon depletion and enhances transistor performance. In addition, the use of metal electrodes with close-to-mid

gap work functions also allows the reduction of substrate doping concentrations, thus enhancing transistor motilities and hence overall transistor performance

Dual epitaxial raised source/drain structure

Through epitaxial deposition, the integrated CMOS tri-gate transistor creates a unique source/drain structure, in which epitaxial deposition of silicon is done for NMOS transistor and Si-Ge for PMOS transistor.

For reducing the parasitic resistance, the source and drain regions are raised with respect to the plane of the gate oxide-silicon substrate interface. This improves device performance. Intel has manufactured prototypes of the integrated tri-gate CMOS transistors on SOI as well as bulk-silicon substrates. The tri-gate transistor on bulk silicon and on SOI demonstrates equivalent scaling and short-channel performance and transistor drive performance.

Researchers found that a process induced vertical compressive strain improves the electron mobility on the sidewall surface with (110) crystal orientation for 3D NMOS, while the conventional embedded Si-Ge source drain stressor can significantly improve the hole mobility on the 110 sidewall for 3D PMOS.

Impact of 3D TRI-Gate Technology and Next Generation FPGAs

The next generation of FPGAs stands poised to benefit from the very latest semiconductor technology to deliver high performance. The primary advantage of Tri-Gate technology to FPGA-based electronic product designer is the continuation of Moore's Law in the steady march of improvements in transistor density, performance, power, and cost-per transistor. Moore's Law is a forecast for the pace of silicon technology development; it states that roughly every 2 years transistor density will double.

FPGAs based on 3D tri-gate technology will deliver dramatic performance gain at low operating voltages. Fig.10 shows that 22nm 3D tri-gate FPGAs will be 37% faster at low voltages than 32nm planar FPGAs. Keeping a constant performance, these FPGAs can operate at lower voltages, hence saving more than 50% of power compared to 32nm planar FPGAs. This makes them ideal for use in small handheld devices, which operate using less energy to "switch" back and forth.

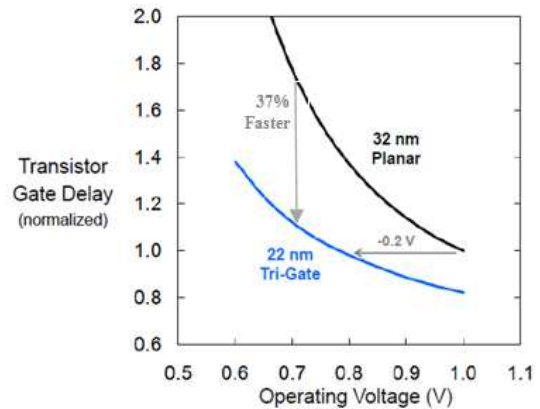


Fig.10 Graph of Transistor Gate Delay vs. Operating Voltage

Fig.11, illustrates the channel current in a Tri-Gate transistor vs. a planar transistor as a function of gate voltage. When the gate voltage is at 0 V, there is an order of magnitude lower amount of leakage current flowing through the channel of the Tri-Gate transistor compared to the planar transistor. Thus the Tri-Gate transistor effectively minimises the leakage power.

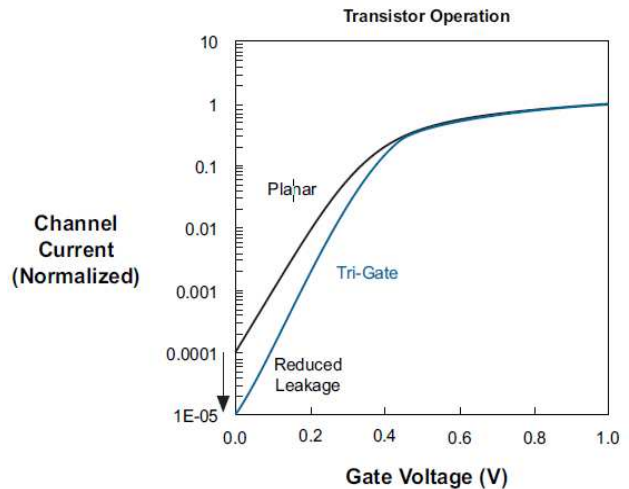


Fig.11 Graph of Channel Current vs. Gate Voltage

Due to lower supply voltage requirement, control over the static and active power dissipation of FPGAs improves tremendously with the 3D tri-gate technology. Figure 12 shows this active power reduction; the trend in active power across process nodes has been in the downward direction. However, as demonstrated by the bend in the curve further downward from the 32 nm planar node, the introduction of Tri-Gate transistors has clearly further reduced the dynamic power beyond the trend established by prior process geometry shrinks.

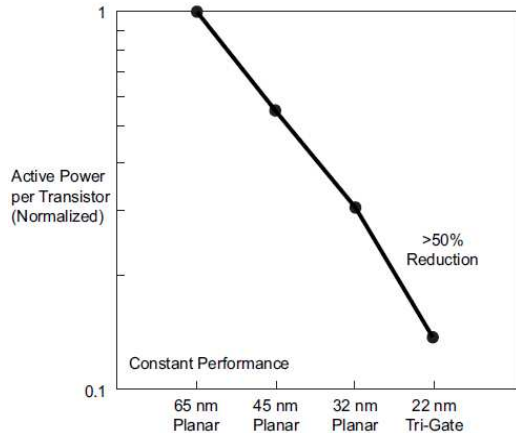


Fig.10 Graph of Active Power in Planar and Tri-Gate Transistors

Other benefits of 3D tri-gate technology on FPGAs includes: improved defect density curves in 22 nm Tri-Gate as compared to 32 nm planar design and reductions in SEU incidence rates from four times to ten times when moving from 32 nm planar to 22 nm Tri-Gate design.

ALTERA Corporation and Intel Corporation have entered into an agreement for the future manufacture of ALTERA FPGAs (e.g. Stratix® 10) on Intel's 14nm tri-gate transistor technology. Next-generation architectures will significantly improve core performance when combined with leading-edge process technology. It would allow for astonishing core speeds of up to 1 GHz. It will bring tremendous improvement in digital signal processing (DSP) capability. Already an area where FPGAs excel, these DSP blocks will become much more efficient in floating-point operations. FPGAs enabled with them will allow for over 10 trillion floating-point operations per second (teraFLOPS) of performance. These will be one of the highest performance, power-efficient solutions at 100 giga floating-point operations per second (GFLOPS) per watt. This would be something unimaginable in existing DSPs or graphics processing units (GPUs). It would allow for breakthrough capabilities in high-performance computing data intensive applications in financial, energy, cloud data analytics, and so on.

Conclusion

3D Tri-Gate technology by Intel is an important innovation needed to continue Moore's Law. This technology when embraced with other semiconductor process technologies like strain engineering, high k/metal gate, Dual epitaxial raised source/drain structure etc. delivers unprecedented performance improvement and power reduction in FPGAs. However, no single

process technology can meet the diverse requirements in end equipment today.

Though 3D Tri-Gate technology will be a foundation of next generation FPGAs to provide the highest core performance at the lowest power, it may not be the optimal solution for everyone. There are other technologies such as TSMC's 20SoC and 55 EmbFlash that can complement Intel's Tri-Gate technology,

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