ABSTRACT
The Phase Locked Loop (PLL) is an almost always used electronics circuit for communication systems like modulator, demodulator, frequency generator and frequency synthesizer etc. All-digital phase locked loop (ADPLL) is digital version of the PLL. In this paper, a novel Hilbert transform based phase detection system for all-digital phase locked loop (ADPLL) is presented. The digital discrete time components are used to realize the phase detector system reducing the complexity of the design. The Hilbert transform based phase detection system provides a definite advantage over conventional analog phase detectors with both sinusoidal and its Quadrature signal. The studied system is modelled and tested in the MATLAB/Simulink environment.

KEYWORD: ADPLL, PLL, Hilbert transform, Phase detector.

INTRODUCTION
With the growth of the wireless communication system, the demand of the stable circuits at high frequency has increased dramatically. The band 2GHz to 4GHz (S band), 4GHz to 8GHz (C band) 8GHz to 12.5GHz (X band) are presently in use for the communication. Hence the compatible electronics is required to use for the generation and detection of wireless signal. To fulfil this requirement, use of the digital component in wireless communication is preferable. Phase-Locked Loop (PLL) is an electronic feedback circuit which is most common circuit for wireless communication system. PLL circuit locks a feedback signal phase relative to input reference signal. It is use to realize the modulator, and demodulator, frequency generator and frequency synthesizer etc. The block diagram of continuous PLL is shown below,

Figure 2: Block diagram of PLL

PLL are classified into various categories as shown in Table 1 [1].

<table>
<thead>
<tr>
<th>PLL</th>
<th>Phase detector or comparator</th>
<th>Loop filter</th>
<th>Voltage or digital controlled oscillator</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog or linear Phase Locked Loop</td>
<td>Analog</td>
<td>Analog</td>
<td>Analog</td>
</tr>
<tr>
<td>Digital Phase Locked Loop</td>
<td>Digital</td>
<td>Analog</td>
<td>Analog</td>
</tr>
<tr>
<td>All Digital Phase Locked Loop</td>
<td>Digital</td>
<td>Digital</td>
<td>Digital</td>
</tr>
</tbody>
</table>

Table 1 Comparison of various types of phase locked loops
This paper focussed on the All-Digital Phase Locked Loop which is a highly demanding component in wireless communication due to its robustness. This is a type of PLL in which all the components are in digital sending and receiving signals in digital form. It can hence be very well realized using FPGA.

Survey on All-digital phase locked loop (ADPLL)

Many researchers have been working in the field of ADPLL. The improved FPGA implementation is the key point of the work. However, researcher also has explored the algorithm improvement. Martin Kumm has presented their work on implementation of ADPLL using FPGA in 2010 [2]. A generic design of digital discrete-time All-digital phase locked loop (ADPLL) using Hilbert transforms and CORDIC method has been realized. This design uses only 15% of FPGA resources. The provides an analytical solution for locking frequency range and stability range. Digital phase locked loop [3] was designed for clock generation in the range of GHz. The bandwidth tracking technique was used to provide stable operation across frequency range without calibration. Chia-Tsun et al. [4] have designed a fast-lock engine to improve lock-in time using Frequency Estimation Algorithm. A 2.4-GHz low power ADPLL was given by Liangge Xu [5]. This All-digital phase locked loop (ADPLL) design is suitable for Industrial, scientific and medical band applications in wireless systems such as wireless local area network (WLAN), Bluetooth and Zigbee where low-power is required. This design, delay based technique is used to reduce TDC power dissipation. Deok-Soo Kim et al. [6] have proposed Adaptive loop gain controller (ALGC) to reduce the non-linearity of bang-bang phase frequency detector and output jitter. In 2011, YoungGun Pu et al. [7] have introduced low power All-digital phase locked loop (ADPLL) having wide range and high resolution Time to Digital converter. In this design, phase interpolator and time amplifier improves the resolution of Time to Digital converter. By using fine resolution of Digital Controlled Oscillator, the phase noise is improved. Xin Chen et al. [8] have designed fast locking All-digital phase locked loop (ADPLL) using feed-forward compensation technique. In this implemented design of All-digital phase locked loop (ADPLL) has two modes: frequency acquisition mode and phase acquisition mode. The fast frequency locking in frequency acquisition mode and linear phase locking in phase acquisition mode is achieved by ADPLL. A digital phase locked loop [9] with Time to Digital converter (TDC) is implemented using a new concept of floating point number representation which is scaled in resolution according to the amount of input difference. The Weining Yin et al. [10] have proposed bandwidth and tuning range technique to reduce jitter and power consumption. Chao-Ching Hung et al. [11] have proposed Bang-Bang Algorithm for fast locking. Davide Tasca et al. [12] have proposed a AO fractional-N Digital Phase Locked Loop based on single bit Time to Digital converter (TDC). In this design, the quantization noise can be cancelled out by placing TDC (digital to time converter) in feedback path and benefits like low noise, low power are achieved.

Digital phase detection using Hilbert transform:

The concept of analytic signal is used in order to obtain the phase information of the signal. The analytic signal as the property that it has no negative frequency components. Any real sinusoid signal can be converted to a positive frequency complex sinusoid by simply generating a phase quadrature component to serve as the imaginary part. For complicated signals consisting of sum of many sinusoids, a filter is used which shifts each component by a quarter cycle. These types of filters are called Hilbert Transform Filters.[13] The analytic signal is generated by applying Hilbert transform to the real signal and using it as the imaginary part to extend the original signal. Let a signal \(v(t)\) is given as

\[
v(t) = \cos(\omega_c t + \theta_e)
\]

Then,

\[
\theta_e = \tan^{-1}\left[\frac{\cos(\omega_c t) \cos(\omega_c t + \theta_e) + \sin(\omega_c t) \sin(\omega_c t + \theta_e)}{\cos(\omega_c t) \sin(\omega_c t + \theta_e) + \sin(\omega_c t) \cos(\omega_c t + \theta_e)}\right]
\]
MATLAB simulation
Two discrete sine wave sources have been used for finding the response of the phase detector. The Simulink diagram of the test bench is shown below.

Figure 4: Simulink Model of phase detector using Hilbert transform
RESULTS
The following parameters have been used for the detection of the signal.

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Frequency of signal</td>
<td>249 MHz and 250 MHz</td>
</tr>
<tr>
<td>2</td>
<td>Sampling Time</td>
<td>0.25 ns</td>
</tr>
<tr>
<td>3</td>
<td>Signal amplitude</td>
<td>1</td>
</tr>
</tbody>
</table>

The model has been simulated for different phases. The detected output for different condition is given below, Phase track for phase difference 5*π/4 (225°).

![Phase detector output with time](image1)

*Figure 6: Phase detector output with time Phase track for phase difference 3*π/4 (135°).*

![Phase detector output with time for phase difference 135°](image2)

*Figure 7: Phase detector output with time for phase difference 135° Phase track for frequency difference of 1 MHz.*
CONCLUSION
The phase detector model has been developed successfully. The maximum three sample clock is required to track the phase. The Simulink results generate the confidence to develop the FPGA block of the phase detector for ADPLL.

REFERENCE